WHAT IS CLAIMED IS:

1. A semiconductor device having a MOSFET, the MOSFET comprising:

source and drain regions formed in a major surface region of a semiconductor substrate;

a gate insulating film formed on a channel region between the source and drain regions;

a gate electrode which is formed on the gate insulating film and includes a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio $\underline{x}$ ($0 < x < 0.2$);

a first metal silicide film which is formed on the gate electrode and essentially consists of $NiSi_{1-y}Ge_y$; and

second and third metal silicide films which are formed on the source and drain regions, respectively, and essentially consist of NiSi.

2. The device according to claim 1, wherein the Ge/(Si+Ge) composition ratio more preferably falls within a range of $0.04 \leqq x \leqq 0.16$.

3. The device according to claim 1, further comprising an interlayer dielectric film which is formed on the MOSFET, a first metal plug which is formed in a first contact hole formed in the interlayer dielectric film on the gate electrode, a first barrier metal layer which is inserted between the first metal plug and the first metal silicide film, second and third metal plugs which are formed in second and third

contact holes formed in the interlayer dielectric film on the source and drain regions, respectively, and second and third barrier metal layers which are inserted between the second and third metal plugs and the second metal silicide film.

4. The device according to claim 3, wherein the first to third metal plugs essentially consist of tungsten, and the first to third barrier metal layers contain TiN.

5. The device according to claim 1, wherein a thickness of the poly-$Si_{1-x}Ge_x$ layer in the gate electrode is at least twice that of the first metal silicide film.

6. The device according to claim 1, which further comprises a well region which is formed in the semiconductor substrate, and in which the source and drain regions are formed in the well region, the source and drain regions have structures with source and drain extensions, and first and second heavily doped impurity diffusion regions and third and fourth lightly doped impurity diffusion regions formed near the channel region in the first and second impurity diffusion regions.

7. A method of manufacturing a semiconductor device, comprising:

forming a gate insulating film on a semiconductor substrate;

forming a gate electrode including a poly-$Si_{1-x}Ge_x$ layer which has a Ge/(Si+Ge) composition ratio $\underline{x}$ ($0 < x < 0.2$) on the gate insulating film;

doping an impurity into a major surface region of the semiconductor substrate to form source and drain regions;

forming an Ni film on the gate electrode and the source and drain regions; and

performing annealing to change the Ni film on the gate electrode into an $NiSi_{1-y}Ge_y$ film and the Ni films on the source and drain regions into NiSi films.

8. The method according to claim 7, wherein the Ge/(Si+Ge) composition ratio more preferably falls within a range of $0.04 \leqq x \leqq 0.16$.

9. The method according to claim 7, further comprising

forming an interlayer dielectric film on the $NiSi_{1-y}Ge_y$ and NiSi films and forming first to third contact holes in the interlayer dielectric film at positions corresponding to the gate electrode and source and drain regions,

forming first to third barrier metal layers in the first to third contact holes, and

burying first to third metal plugs on the first to third barrier metal layers in the first to third contact holes.

10. The method according to claim 7, further

comprising, before formation of the gate insulating film,

forming an element isolation structure on the major surface of the semiconductor substrate, and

forming a well region in an active element region defined by the element isolation structure.

11. The method according to claim 7, wherein formation of the source and drain regions includes

ion-implanting an impurity into the major surface region of the semiconductor substrate using the gate electrode as a mask to form first and second lightly doped impurity diffusion regions,

forming sidewall insulating films on sidewall portions of the gate electrode, and

ion-implanting an impurity into the major surface region of the semiconductor substrate using the gate electrode and the sidewall insulating films as a mask to form third and fourth heavily doped impurity diffusion regions.

12. The method according to claim 9, wherein formation of the interlayer dielectric film includes

depositing a silicon nitride film on the major surface of the semiconductor substrate and upper and side surfaces of the gate electrode, and

depositing a silicon oxide film on the silicon nitride film.

13. The method according to claim 9, wherein

formation of the first to third barrier metal layers includes

forming a Ti film on the interlayer dielectric film and in the first to third contact holes, and

nitriding the Ti film to convert at least part of the Ti film into a TiN film.

14. The method according to claim 9, wherein burying of the first and third metal plugs includes

forming a tungsten layer on the lightly doped impurity diffusion regions and in the first to third contact holes by CVD, and

executing CMP to planarize the surface and leaving the tungsten layer in the first to third contact holes to form the first to third metal plugs.